Vorne Industries

2000B Series
Buffered Display
Users Manual

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2000B Series Buffered Display
Release 1.1

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1. INTRODUCTION

1.1 General Introduction

The Vorne 2000 series alpha numeric buffered display is a single board module which combines a 20 character (dot matrix) vacuum fluorescent display tube, voltage converter and display controller in one package to provide a complete and simple to use buffered display system. Only one 5 volt source is required, and the internal display controller executes all timing, control, refresh and character generation functions. A full ASCII set of 128 characters is supported by the display controller. The buffered display easily interfaces to any host processor which can provide data (8 bit control or character words) in the specified series or parallel 8 bit format. Control words allow adjustment of various display parameters (brightness, refresh rate, etc.) and the implementation of features such as scrolled messages, a blinking cursor, etc. The display characters have a wide viewing angle and are a bright blue green color (filterable to blue, green, red or yellow).

1.2 Structure of Manual

This manual is split into two sections. The first section describes the hardware interface to the buffered display and includes electrical characteristics, timing requirements, and wiring diagrams. The second section describes the software interface to the display — how to load characters, utilize control parameters, initialize the display controller, etc.

2. HARDWARE INTERFACE TO THE BUFFERED DISPLAY

2.1 Electrical Characteristics

The input lines to the buffered display consist of:
1) Supply voltages (either 5 Volt DC, 10-30 Volt DC or 120 Volt AC)
2) POR (Power on reset)
3) LD (Data load strobe)
4) D0-D7 (8 bit data port)

The current and power requirements (maximum) necessary to operate the buffered display are listed below, for the 5 volt DC, 10-30 volt DC and 120 volt AC versions.

MODEL	5 VOLT DC +- 5%	10-30 VOLT DC	120 VOLT AC +- 15%
2005B	275 Milliamps	140-50 Milliamps	5 Volt-Amps
2009B	460 Milliamps	230-80 Milliamps	10 Volt-Amps
2015B	1000 Milliamps	500-170 Milliamps	15 Volt-Amps

All other lines (POR, LD, D0-D7) respond to logic levels with the voltage characteristics listed below:

STATE	MIN	MAX
Logic 0	-1.0 Volts	0.8 Volts
Logic 1	3.8 Volts	5.3 Volts

2.2 Schmitt Trigger Inputs

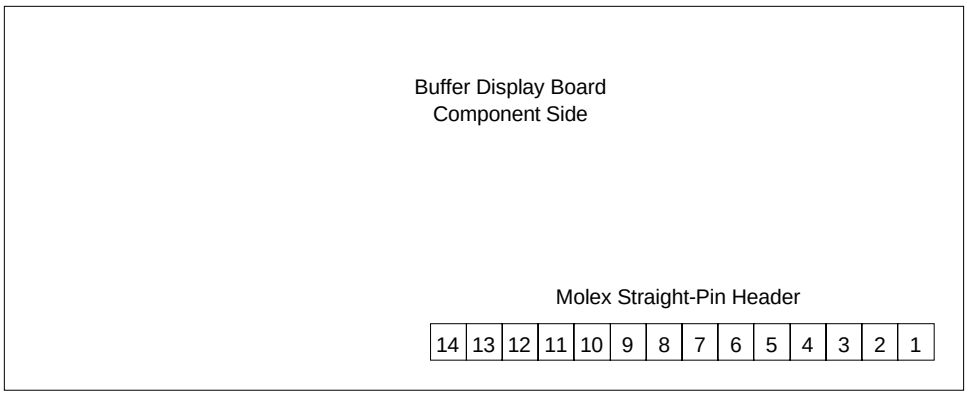
In applications where the host processor is located more than a few inches away from the buffered display there is the potential for transients and electrical noise to interfere with normal operation of the display. In applications where electrical noise is a potential problem, it is recommended that the optional Schmitt trigger input board be used to interface the buffer display with the host processor. The only operational difference resulting from using this board is that timing requirements are slightly different as RC filtering is used to further eliminate electrical transients. The timing charts show timing value differences for operation with the Schmitt trigger input board.

2.3 Wiring Diagrams

Depending on the particular options chosen for the buffered display, one of five wiring diagrams needs to be referenced. All three sizes of the buffered display have the exact same wiring. Options that affect wiring are the input voltage chosen (5 volt DC, 10-30 volt DC or 120 volt AC), whether or not a case is provided (case models are wired via 2 electrovert terminal strips; other models through a 14 position, single row, .1 inch center, .025 square male pins), and whether the input is direct or through a Schmitt trigger board. All possible variations and their respective wiring diagrams are shown below. Terminal and pin designations are consistent throughout the series.

SUPPLY VOLTAGE	HOUSING	INPUT TYPE	WIRING DIAGRAM
5 Volt DC	No case	Direct	Figure 1A
5 Volt DC	No case	Schmitt trigger	Figure 1B
5 Volt DC	Panel mount case	Direct	Figure 2A
5 Volt DC	Panel mount case	Schmitt trigger	Figure 2A
10-30 Volt DC	Panel mount case	Direct	Figure 2B
10-30 Volt DC	Panel mount case	Schmitt trigger	Figure 2B
120 Volt AC	Panel mount case	Direct	Figure 2C
120 Volt AC	Panel mount case	Schmitt trigger	Figure 2C

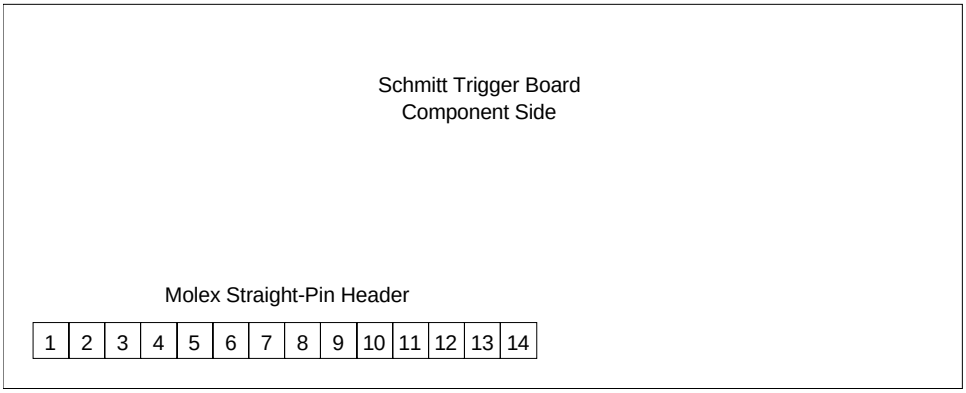
Figure 1A
5VDC - Direct Input - No Case



Connections

1) +5VDC IN
2) GND IN
3) N.C.
4) N.C.
5) POR
6) LD
7) D0
8) D1
9) D2
10) D3
11) D4
12) D5
13) D6
14) D7

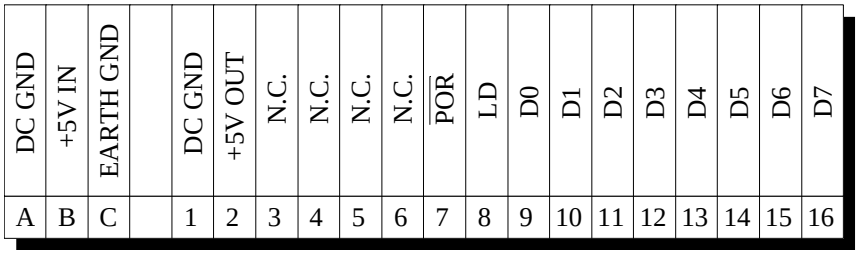
Figure 1B
5VDC - Schmitt Trigger Input - No Case



Connections

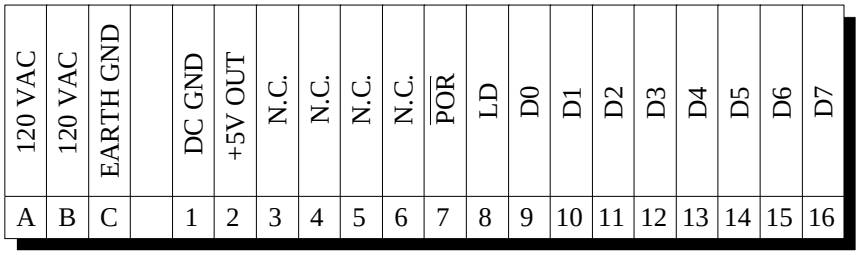
1) +5VDC IN
2) GND IN
3) N.C.
4) N.C.
5) POR
6) LD
7) D0
8) D1
9) D2
10) D3
11) D4
12) D5
13) D6
14) D7

Figure 2A
5VDC - Panel Mount Case



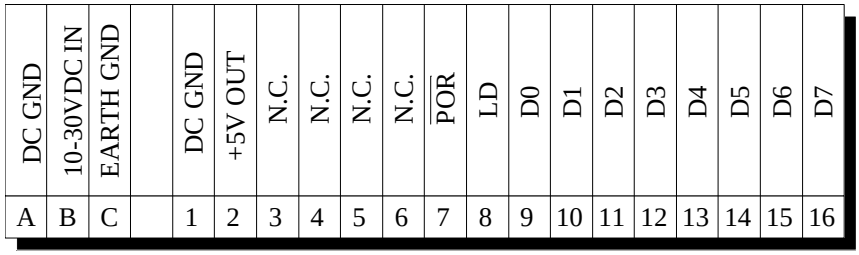
DC GND	+5V IN	EARTH GND		DC GND	+5V OUT	N.C.	N.C.	N.C.	N.C.	$\overline{\text{POR}}$	LD	D0	D1	D2	D3	D4	D5	D6	D7
A	B	C		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Figure 2C
120VAC - Panel Mount Case



120 VAC	120 VAC	EARTH GND		DC GND	+5V OUT	N.C.	N.C.	N.C.	N.C.	$\overline{\text{POR}}$	LD	D0	D1	D2	D3	D4	D5	D6	D7
A	B	C		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Figure 2B
10-30VDC - Panel Mount Case



DC GND	10-30VDC IN	EARTH GND		DC GND	+5V OUT	N.C.	N.C.	N.C.	N.C.	$\overline{\text{POR}}$	LD	D0	D1	D2	D3	D4	D5	D6	D7
A	B	C		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

2.4 Operation Summary

The power on reset (POR) line initializes the internal circuits of the display controller, and sets various software and hardware controlled parameters to initial states (see power on reset in section 3.3). The data load strobe (LD) informs the display controller that a new control or character word is ready to be loaded. The 8 bit data port (D0 - D7) can function in a parallel mode (using all 8 data lines) or a serial mode (using D0 as the data line and D1 as a serial clock).

2.5 Serial Interface

In serial mode only lines D0 and D1 of the data port are used. D0 is the data line and D1 is the serial clock. The display controller uses an internal shift register to accumulate 8 bits of information (a full word). Data must be input MSB (most significant bit) down to LSB. When eight bits have been shifted in, the LD line is strobed to load the data. Timing waveforms for serial interface are shown in Figure 3A. When power is first applied to the display, or the POR line is strobed, the display is initially set to the serial mode. The parallel mode is activated by toggling any of the lines D2 - D7, when the buffered display is used exclusively in the serial mode these lines should be tied to ground.

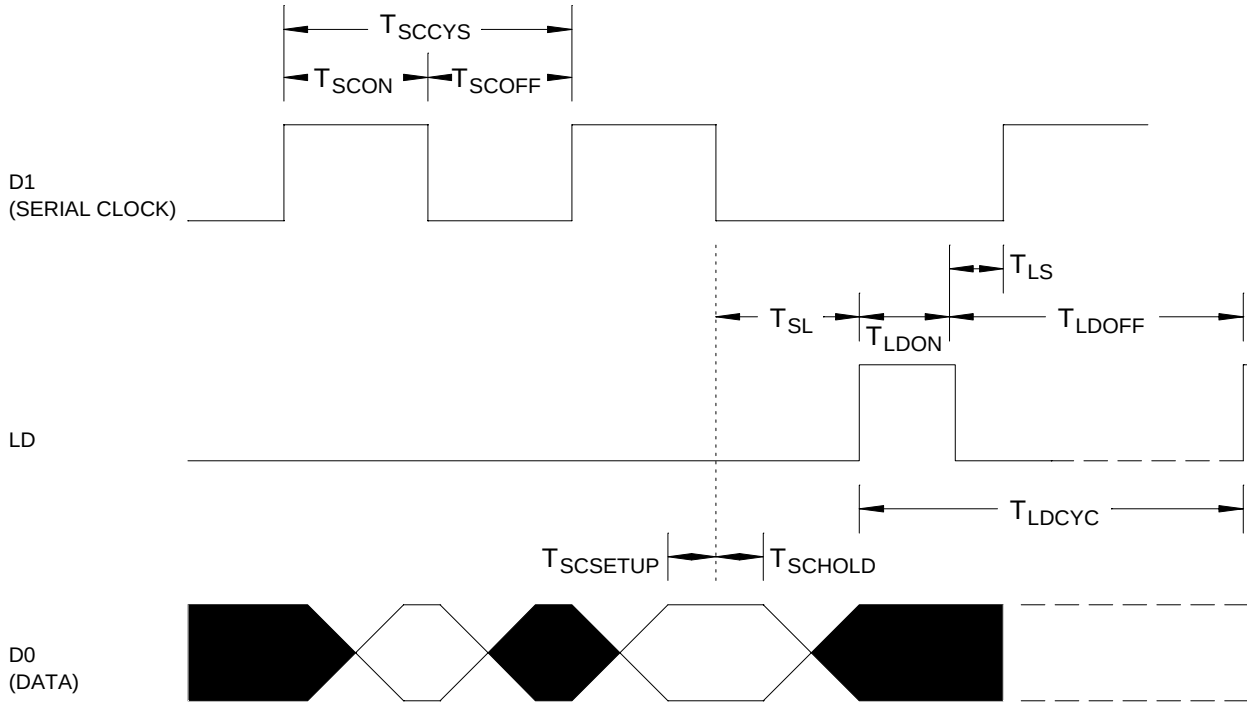


Figure 3A
Serial Interface Timing Waveforms

SCHMITT TRIGGER	DIRECT
2	2 µS ≤ T_{SCCYS}
1	1 µS ≤ T_{SCON} ≤ 20 µS
1	1 µS ≤ T_{SCOFF}
1	1 µS ≤ $T_{SCSETUP}$
1	1 µS ≤ T_{SCHOLD}
50	1 µS ≤ T_{LDON}
50	40 µS ≤ T_{LDOFF}
100	60 µS ≤ T_{LDCYC}
1	1 µS ≤ T_{LS}
1	1 µS ≤ T_{SL}

2.6 Parallel Interface

In parallel mode the entire 8 line data port (D0 - D7) is used to receive data. The most significant bit of this port is D7; the least significant bit is D0. When the LD line is strobed, data on the port will be loaded into the display controller. Timing waveforms for parallel interface are shown in Figure 3B. When power is applied to the display, or the POR line is strobed, the display is initially set to the serial mode. To activate the parallel mode, it is necessary as part of an initialization procedure to toggle any or all of the lines D2 - D7. After this has been done, the display will be in the parallel mode until a new POR.

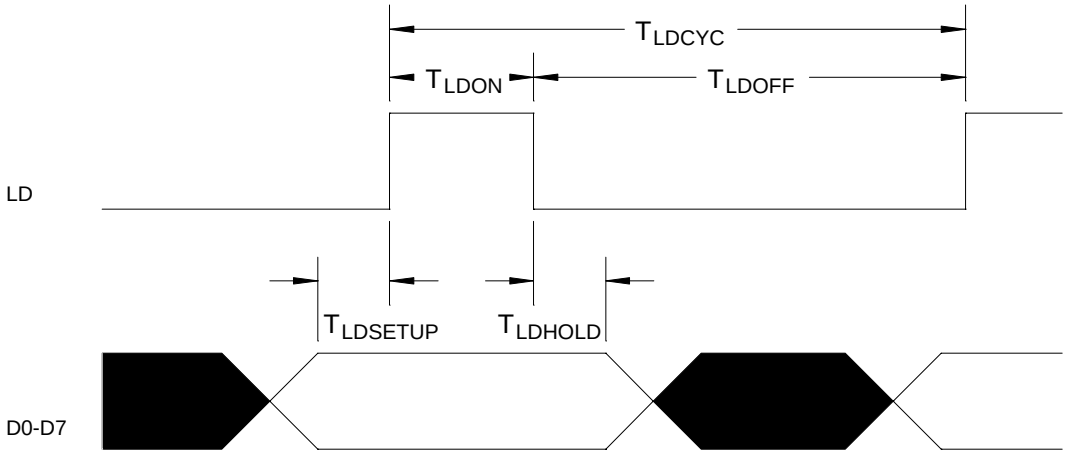


Figure 3B
Parallel Interface Timing Waveforms

SCHMITT TRIGGER	DIRECT
50	40 µS ≤ T_{LDOFF}
50	1 µS ≤ T_{LDON}
0	0 µS ≤ $T_{LDSETUP}$
1	1 µS ≤ T_{LDHOLD}
100	60 µS ≤ T_{LDCYC}

3. SOFTWARE INTERFACE TO THE BUFFERED DISPLAY

3.1 Theory of Operation

The display controller maintains a twenty character display buffer, the contents of which are continually displayed on the VFD tube. To stop the display process it is necessary to apply a signal to the POR line (10 millisecond minimum duration low, followed by 10 millisecond high; then hold high until the next POR). After POR the display controller will accept all commands, but will not display anything until a special control word is input (the start refresh command), which begins the display refresh cycle. In summary, the display tube will always reflect the contents of the display buffer — except for the interval between a POR (power on reset) and a start refresh command (software command - control word 0E Hex).

3.2 Software Commands

Two types of data can be loaded through the data port. The first is character data, specified by the standard seven bit ASCII code (reproduced in the Appendix). The eighth (MSB) bit is also used as a control bit to enable blanking or inverse video display of flagged characters (as is described below). The second type of data used is control words. Control commands are loaded as a sequence of two words. The first is always 01 which is the control prefix specifying that the next data is to be interpreted as a control command, which will fall under one of the following catagories:

1) Setting the display mode
2) Setting the digit counter
3) Setting the buffer pointer register
4) Setting the digit time
5) Setting the duty cycle
6) Starting the display refresh cycle

Control Word Assignments

Hex Value	Function
01	Load 01
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is ignored)
09	Enable Blank Mode (data words with MSB = 1 will be blanked)
0A	Enable Inverse Mode (data words with MSB = 1 will be inverted)
0E	Start Display Refresh Cycle (use only once after reset)
40-7F	Load Duty Cycle Register
81-94	Load Digit Counter
C0-D3	Load Buffer Pointer Register

TABLE 1

1) SETTING THE DISPLAY MODE

COMMAND	FUNCTION
08 Hex	Enable normal display mode (MSB in character words is ignored).
09 Hex	Enable blank mode (character words with MSB=1 will be blanked).
0A Hex	Enable inverse mode (character words with MSB=1 will be “inversed”).

Only seven bits are necessary to represent a full ASCII set of 128 characters. The eighth (most significant) bit of character words is used, however, to signify special treatment of characters under certain conditions. The display can be selected for three different modes (normal, blank and inverse) through control words 08 - 0A Hex. When in the normal display mode, all characters in the display buffer are displayed without modification (the eighth bit is ignored). When in the blank display mode, all characters with an MSB (most significant bit) of one are blanked (not displayed). When in the inverse mode, all characters with an MSB of one are displayed in an “inverse video” type format.

2) SETTING THE DIGIT COUNTER

COMMAND	FUNCTION	
81-94 Hex	Set Digit Counter	See TABLE 2

The digit counter defines the number of character positions to be displayed. Note that although this would normally be set at twenty (for the twenty characters of the VFD tube) it is possible to set it to a lesser number in order to use a smaller area of the display (eg. 10 characters). The displayed portion will always begin with the first character of the left side of the display tube (the most significant character).

Load Digit Counter Codes

Code	No. of Grids Controlled
81	1
82	2
83	3
84	4
85	5
86	6
87	7
88	8
89	9
8A	10
8B	11
8C	12
8D	13
8E	14
8F	15
90	16
91	17
92	18
93	19
94	20

TABLE 2

3) SETTING THE BUFFER POINTER REGISTER

COMMAND	FUNCTION
C0-D3 Hex	Set Buffer Pointer Register See TABLE 3

The buffer pointer register holds the current value of the buffer pointer. After each character is loaded, the buffer pointer register is automatically incremented and points to the next character position; thus, an entire string of 20 characters can be sequentially loaded by merely loading the 20 ASCII character codes. When the buffer pointer is equal in value to the digit counter, it automatically resets to character position 1 (the most significant or leftmost character when viewing the display). The buffer pointer register can be directly set to any of the twenty character positions by utilizing the Set Buffer Pointer Register commands. This allows complete random access to the entire display buffer.

Duty Cycle Control Codes

Code	Digit Time=16		Digit Time=32		Digit Time=64	
	On	Off	On	Off	On	Off
40	-	16	-	32	-	64
41	-	16	-	32	-	64
42	-	16	-	32	-	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
5D	"	"	27	5	27	37
5E	"	"	28	4	28	36
5F	"	"	29	3	29	35
60	"	"	29	3	30	34
.	"	"	29	3	31	33
.	"	"	"	"	32	32
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	"	"	"	"	58	6
7D	"	"	"	"	59	5
7E	"	"	"	"	60	4
7F	"	"	"	"	61	3

TABLE 3

4) SETTING THE DIGIT TIME

COMMAND	FUNCTION
05 Hex	Set digit time to 16 cycles per character.
06 Hex	Set digit time to 32 cycles per character.
07 Hex	Set digit time to 64 cycles per character.

The digit time codes set the time alloted for each character during the refresh cycle. The default setting after a power-on reset is 64 cycles per character. Under conditions where the display may be subjected to quick movements during viewing, it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid, with the appropriate control code.

5) SETTING THE DUTY CYCLE

COMMAND	FUNCTION	
40-7F Hex	Set Duty Cycle	See TABLE 4

Control codes 40-7F Hex offer different duty cycle combinations. Note that the duty cycle is dependent on the digit time value chosen. In all cases control words 40-42 turn the display off. Thus, duty cycle settings can be used to turn the entire display on and off. Control over the duty cycle also allows user variation of the display brightness. The larger the "on time", the brighter the display will be.

Load Buffer Pointer Codes

Code Value	Character Position
C0	1
C1	2
C2	3
C3	4
C4	5
C5	6
C6	7
C7	8
C8	9
C9	10
CA	11
CB	12
CC	13
CD	14
CE	15
CF	16
D0	17
D1	18
D2	19
D3	20

TABLE 4

6) STARTING THE DISPLAY REFRESH CYCLE

COMMAND	FUNCTION
0E Hex	Start Display Refresh Cycle

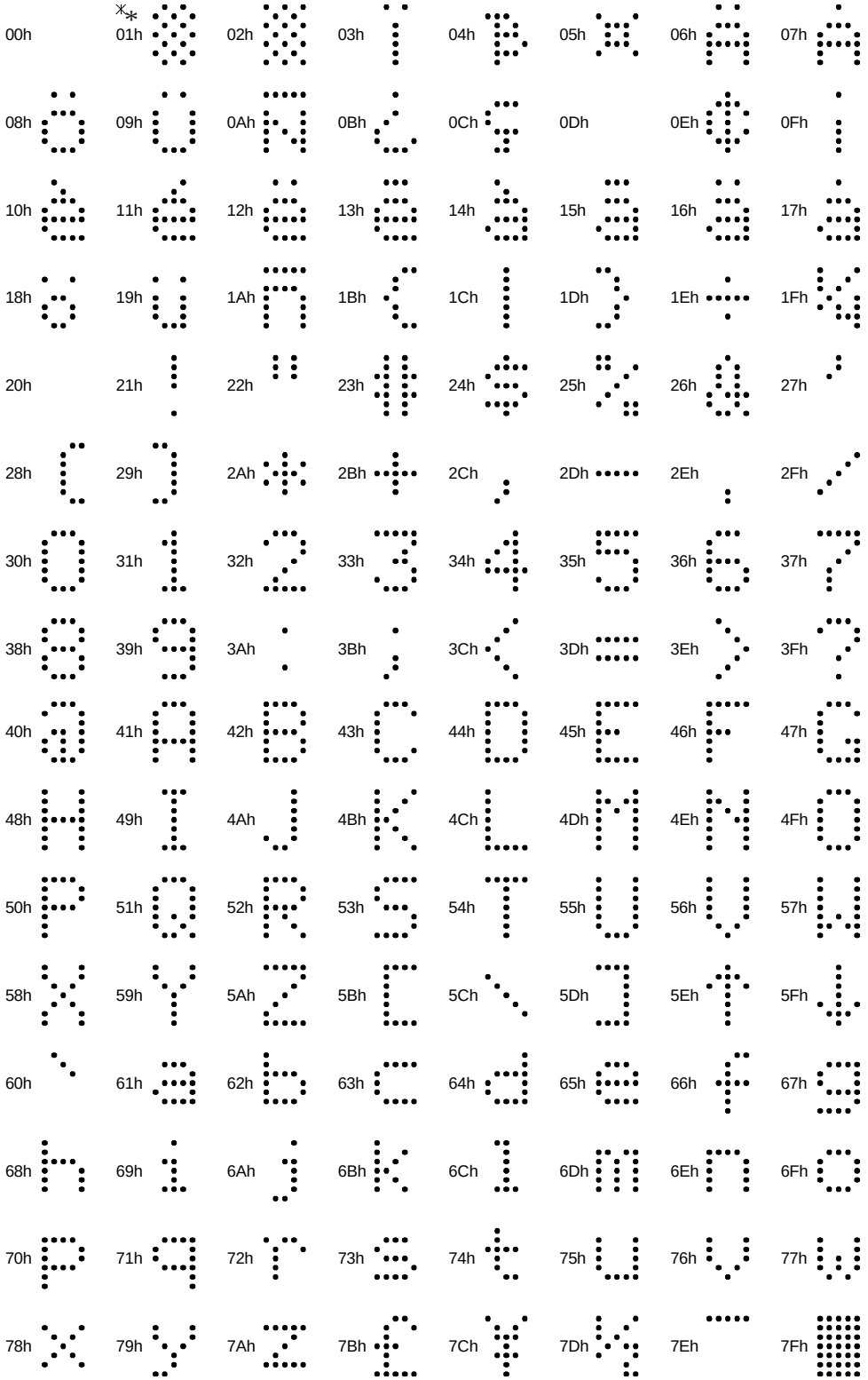
After a POR (power on reset) the display controller will remain in an internal hold mode, not driving the VFD tube until the start display refresh cycle command code is applied. While on internal hold, control words can be loaded and the data buffer can be filled. Since there is no display driving, no "garbage" will be seen on the display tube. Display driving begins only after the control word for the start display refresh cycle has been loaded, and will continue until a new POR or loss of power.

3.3 Power-on Reset

To stop the display process it is necessary to apply a signal to the POR line (10 millisecond minimum duration low, followed by 10 millisecond high; then hold high until the next POR). After POR the display controller will accept all commands, but will not display anything until a special control word is input, which begins the display refresh cycle. Strobing the POR line also initializes the internal circuits of the display controller, and sets various software controlled parameters to the following initial states.

1) The VFD tube is held off.
2) Duty cycle is set to 0. (Code 40 Hex)
3) The digit counter is set to zero.
4)The buffer pointer is set to character position1. (Code C0 Hex)
5) Digit time is set to 64. (Code 07 Hex)
6) The Normal display mode is set. (Code 08 Hex)
7) The display is set to accept serial input.

4. APPENDIX
Character Set



* Since the value 01 hex represents both a command prefix and a character pattern, the sequence 01 01 loads the character pattern for 01 into the data buffer.

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